CLAIMS

What is claimed is:

1. A bipolar transistor comprising:

a base region comprising an intrinsic base region and surrounding raised extrinsic base regions;

a block polysilicon emitter region located atop and in contact with said intrinsic base region;

a first silicide layer located on the raised extrinsic base region, said first silicide layer having an inner edge that is self-aligned to the block polysilicon emitter region;

a second silicide layer located in the block polysilicon emitter region, said second silicide layer is self-aligned to the first silicide layer; and

a self-aligned emitter contact border located atop the raised extrinsic base region.

2. The bipolar transistor of Claim 1 wherein the second silicide layer is located atop a polysilicon emitter.

3. The bipolar transistor of Claim 1 wherein the second silicide layer is located inside said block polysilicon emitter region and atop a conformal polysilicon emitter.

4. The bipolar transistor of Claim 1 wherein the block polysilicon emitter region includes an emitter polysilicon that has an upper surface that is above an upper surface of the raised extrinsic base.

5. The bipolar transistor of Claim 1 wherein the self-aligned emitter contact border is defined by a spacer.

6. The bipolar transistor of Claim 5 wherein the spacer provides isolation between said base region and a polysilicon emitter of the block polysilicon emitter region.

7. The bipolar transistor of Claim 5 wherein the spacer is a wide spacer, a double spacer or an L-shaped spacer.

8. The bipolar transistor of Claim 1 wherein said block polysilicon emitter region includes insulating spacers that define the emitter's final dimension and provide lateral emitter-base isolation.

9. The bipolar transistor of Claim 1 further comprising an emitter contact located directed atop the self-aligned emitter contact border and the block polysilicon emitter region.

10. The bipolar transistor of Claim 9 wherein the emitter contact has a dimension that is larger than a dimension of block polysilicon emitter region.

11. The bipolar transistor of Claim 1 further comprising a base contact located directly atop the raised extrinsic base region.

12. The bipolar transistor of Claim 1 further comprising a silicided collector reach-through region located in a surface of a Si-containing substrate that underlies said transistor.

13. The bipolar transistor of Claim 12 further comprising a collector contact atop said silicided collector reach-through region.

14. A bipolar transistor comprising

a base region comprising an intrinsic base region and surrounding raised extrinsic base regions;

a block polysilicon emitter region located atop and in contact with said intrinsic base region;

a silicide layer located on the raised extrinsic base region, said silicide layer having an inner edge that is self-aligned to the block polysilicon emitter region; and

a self-aligned emitter contact border located atop the raised extrinsic base region.

15. The bipolar transistor of Claim 14 wherein the block polysilicon emitter region includes a recessed emitter polysilicon that has an upper surface that includes a metallic plug thereon.

16. The bipolar transistor of Claim 14 wherein the block polysilicon emitter region includes a recessed emitter polysilicon that has an upper surface that is contact with an overlying emitter contact.

17. The bipolar transistor of Claim 14 wherein the self-aligned emitter contact border is defined by a spacer.

18. The bipolar transistor of Claim 17 wherein the spacer provides isolation between said base region and a polysilicon emitter of the block polysilicon emitter region.

19. The bipolar transistor of Claim 17 wherein the spacer is a wide spacer, a double spacer or an L-shaped spacer.

20. The bipolar transistor of Claim 14 wherein said block polysilicon emitter region includes insulating spacers that define the emitter's final dimension and provide lateral emitter-base isolation.

21. The bipolar transistor of Claim 14 further comprising an emitter contact located directed atop the self-aligned emitter contact border and the block polysilicon emitter region.

22. The bipolar transistor of Claim 21 wherein the emitter contact has a dimension that is larger than a dimension of block polysilicon emitter region.

23. The bipolar transistor of Claim 14 further comprising a base contact located directed atop the raised extrinsic base region.

24. The bipolar transistor of Claim 14 further comprising a collector reach-through region located in a surface of a Si-containing substrate that underlies said transistor.

25. The bipolar transistor of Claim 24 wherein the collector reach-through region is silicided

26. The bipolar transistor of Claim 25 further comprising a collector contact atop said silicided collector reach-through region.

27. A method of fabricating a bipolar transistor comprising the steps of:

forming an emitter opening in a raised extrinsic base/dielectric stack, said emitter opening having an insulating spacer therein that defines the emitter's final dimension and provides lateral emitter-base isolation;

providing a block polysilicon emitter region in said emitter opening;

removing said dielectric to expose said raised extrinsic base;

patterning said exposed raised extrinsic base;

forming a first silicide layer on at least said patterned raised extrinsic base, said first silicide layer having an inner edge that is self-aligned to the block polysilicon emitter region; and

forming a self-aligned emitter contact border atop a portion of the patterned raised extrinsic base.

28. The method of Claim 27 further comprising forming a second silicide layer on a surface of a polysilicon emitter located in said block polysilicon emitter region.